Digital Combiner Interconnect Definition

The register set is designed as a typical 32-bit, four-byte addressable system. Each byte has an active high write enable (WR[3:0]) with WR3 enabling the MSB, WR0 the LSB. CS needs to be high for any reads or writes. The five-bit address bus determines which register to access.

# Register 0 Default x”0C80”

Register 0 is 32 bits and comprises the 18-bit unsigned Lag coefficient in bits [17:0].

When read, lock information is stuffed into the upper 4 bits as {‘0’, realLock, imagLock, locked}. realLock implies the two real inputs are correlated. Likewise, imagLock implies the imaginary parts are correlated. Note that for a BPSK signal, the imaginary part is usually zero, however the combiner doesn’t require the IFs to be phase locked by a demod and the IF will rotate at the beat frequency.

There's a Real and an Imaginary lock counter since the signal can disappear on one leg during a beat note, so we check both legs independently. The Lock counter increments by one to 8191 when the two real MSBs are equal but decrements by two otherwise. If there's no signal, the count usually hovers around 100, but occasionally peaks above 128, so we set the threshold at 128 then add/subtract 112 for hysteresis such that both signals have to drop below 16 to lose lock, then either must rise above 240 to regain lock. This gives a strong confidence to the lock and allows the 8192 a long time (76uS) to count down to 256 during a fade.

Note, the higher the beat note in the IF, the more “false negatives” at high noise levels. At 800Hz offset, I've seen an error every 10 seconds or so.

# Register 4 Default = x”A000”

Register 4 is 32 bits and comprises the 18-bit unsigned Lead coefficient in bits [17:0].

When read, the correlation index is stuffed into the upper 8 bits (31:24) as a signed value. Positive implies IF1 arrived before IF2. As the combiner time aligns the two IFs, the index will go to zero.

# Register 8 Sweep Rate Default = x”0064”

Sweep Rate determines how fast the frequency offset is swept trying to force the phase detector into the lock range of the combiner. Sweep Rate is disabled when Lock is declared. The value is an 18-bit unsigned number.

# Register C Sweep Limit Default = 20KHz

Combiner sweep limit is a 16-bit register using only 14 LSBs. The data must reside in bytes 1 and 0.

The 14-bit number limits the range of the combiner sweep circuit. The value equals LimitInHz / SystemClock \* 2^22.

# Register D Options Default = 0

There are two bits used in this 16-bit register. The data must reside in bytes 3 and 2.

Bit 0 sets the ifBS\_n output which is used in the Semco demods for enabling the combined IF back to 70MHz.

Bit 4 enables the combiner. It acts as a soft reset when low.

# Register x10 Combiner Lock Threshold and Hysteresis. Default 0x800700

The Lock Threshold is bits 28 to 16 with Hysteresis in bit 15 to 4, so the default above gives 80 and 70 for the two values.

The 2:0 bits are test options. Usually set to 0.

Bit 0 disables the high frequency AM compensation. This accounts for any AM signals not removed with the AGC, such as fast fades.

Bit 2 overrides the Ch1GtCh2 comparator with the value in Bit 1. Used for testing the combiner.

# General Information

If either input signal is below threshold, the BestSource output goes high and the larger of the two channels is output as a BestSource switch.

In our system, the Channel 1 and Channel 2 AGC voltages from the IFs are ±2V over an 80dB range. +2 is very strong, -2 is 80dB down. The AGCs are sent to a 12-bit A/D with a 3.3V range. The input is resistively scaled from ±2.0V to ±1.5V (3Vpp) centered at 1.65V. Since we are only using 3/3.3=90.9% of the available A/D range and the digital inputs are in 12.11 format for ±1.0, the input signal range is ±0.909V to cover ±40dB.

Note that the required range is 80dB, but the headroom of the A/D gives us an actual range of 80\*3.3/3 = 88dB or ±44dB. This is beneficial as shown below.

We take the difference in AGC voltage between the two channels to define the weighting system based on the stronger signals. If we take the differential and multiply by 4 with saturation this effectively gives us a ±11dB differential maximum. We can use this to limit the range the combiner attempts to work over since combining is only useful over a 10dB range. The nature of the saturation forces a "Best Source Select" function automatically. The difference value addresses a look up table that does the log to linear conversion over a 16384-bit resolution. The Log2Lin transposes the log nature of the AGC to a linear ratio of the two signals. If the two AGCs are the same, the differential is zero and the weights are set to 50-50 for optimal combining. As the difference approaches +1.0, the largest signal gets a weight of 100%.and the other is shut off with a weight of 0%.

# I/O Definitions

The top level module is called “DigitalCombiner” with the following signals. Note, the combiner determines the maximum (Max) of the two channels and phase locks the minimum (Min) channel to it. The top level is written in VHDL, so the table uses that syntax to define the signal width and sign. I took some liberties with the verbosity such as STD\_LOGIC\_VECTOR => SLV and “downto” is just “:”.

|  |  |  |
| --- | --- | --- |
| Clk | IN STD\_LOGIC | Symbol Rate Clock, usually 46.6MHz |
| clk2x | IN STD\_LOGIC | Twice symbol rate, used for reconstructed IF output |
| clk4x | IN STD\_LOGIC | Four times symbol rate for FFTs and processing |
| reset | IN STD\_LOGIC | Active high reset |
| ce | IN STD\_LOGIC | Active high clock enable, usually set to ‘1’ |
| busClk | IN STD\_LOGIC | Processor clock |
| cs | IN STD\_LOGIC | Processor chip select, active high |
| wr0, wr1, wr2, wr3 | IN STD\_LOGIC | Byte write enables, wr3 is 31:24 |
| addr | IN SLV(4:0) | 5 bit processor address |
| dataIn | IN SLV32 | 32 bit processor write data bus |
| dataOut | OUT SLV32 | 32 bit processor read data bus |
| re1In, im1In, re2In, im2In | IN sfixed(0:-17) | 18 bit signed Real and Imaginary inputs from channel 1 and 2 |
| ch1agc, ch2agc | IN sfixed(0:-11) | 12 bit signed AGC voltages |
| imagout, realout | OUT sfixed(0:-17) | 18 bit signed Combined I/Q outputs. |
| ifOut | OUT sfixed(0:-17) | 18 bit signed Reconstructed Combined IF output at 2x clock rate |
| agc1\_gt\_agc2 | OUT STD\_LOGIC | Indicates which channel is the maximum. The minimum is phase locked to the maximum |
| locked | OUT STD\_LOGIC | Lock detector output |
| bestSource | OUT STD\_LOGIC | Combining has insufficient SNR and resorts to a switch |
| combinerEn | OUT STD\_LOGIC | Combiner is active when high. Tied to Options register |
| The signals in *Italics* are test points and not expected to be used | | |
| *realxord, imagxord* | *OUT STD\_LOGIC* | *Real MSBs and Imag MSBs XOR’d for the lock detector* |
| *ifBS\_n* | *OUT STD\_LOGIC* | *Options register output* |
| *imaglock, reallock* | *OUT SLV(12:0)* | *Lock detector counter outputs* |
| *maximagout, maxrealout, minimagout, minrealout* | *OUT sfixed(0:-17)* | *I/Q outputs of the max and min channels. No processing has been done, just a crossover switch.* |
| *gainoutmax, gainoutmin* | *OUT sfixed(0:-17)* | *Combiner weights for the Maximum and minimum channels* |
| *phase\_detect* | *OUT sfixed(0:-17)* | *Phase Detector output* |
| *lag\_out* | *OUT SLV32* | *Lag and Sweep adjusted phase detector output* |
| *nco\_control\_out* | *OUT SLV(21:0)* | *Lead adjusted and negated Lag Out depending of Agc1GtAgc2* |